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No. 0068 P. 1

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October 4, 2005

Via Facsimile 571-273-8300

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Re: Serial No.: 09/738,193  
Art Unit: 2827  
Examiner: David E. Graybill  
System, Method and Apparatus for Constructing a Semiconductor Wafer-Interposer Using B-Stage Laminates  
Our File: 1384-1023

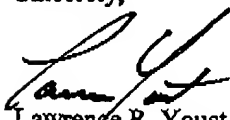
Dear Sir:

Enclosed for filing please find the following items relating (4 + 1 pages) to the above-identified application:

- (1) Petition to Revive Unintentionally-Abandoned Application (2 pages);
- (2) Request for Continued Examination (1 page); and
- (3) Form PTO-2038 authorizing a payment in the amount of \$1145.00 (1 page).

If you have any questions or comments concerning this matter, please call the undersigned at your earliest convenience. Otherwise, please accept the enclosed.

Sincerely,

  
Lawrence R. Youst  
Reg. No. 38,795

Enclosures

Certificate of Transmission Under 37 C.F.R. §1.8

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on October 4, 2005.

  
Lawrence R. Youst

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